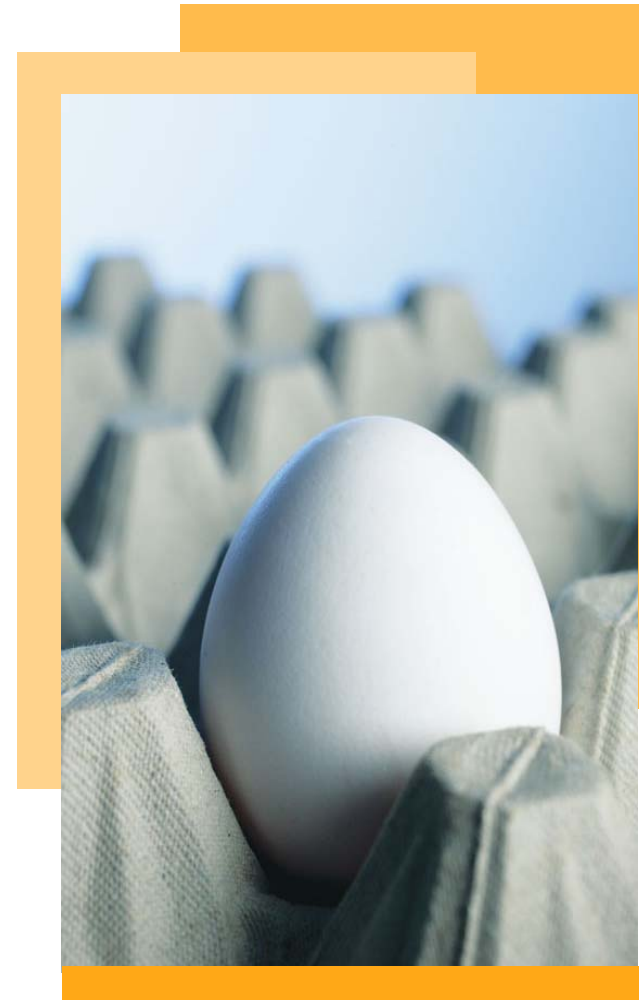


Hardware BOSS

Friedrich Schön
Abteilungsleiter Eingebettete Systeme
2nd TET Customer Day, Munich, 5.7.2010



Fraunhofer FIRST - Facts

**Your Technology Partner in Southeastern Berlin
for Computer Architecture and Software
Technology!**

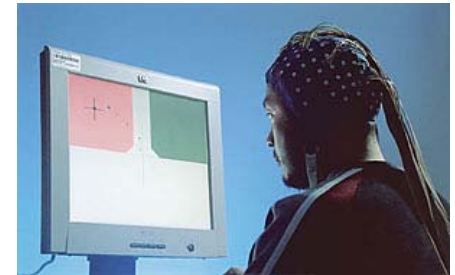
- Founded in 1983 as a GMD Institute
 - Focus: Computer Architecture
 - Institute Head: Prof. Wolfgang Giloi
- Expansion in the 90s; Added new groups
 - Focus: Software Technology
 - Institute Head: Prof. Stefan Jähnichen
- Since 2001, Member Institute, Fraunhofer Society
- 3 Departments, ca. 130 staff, about 85 researchers



Fraunhofer FIRST – Structure

High End Technology for your Applications

- Interactive Systems (ISY)
 - *Visualization Technologies*: Dome Projection, Digital Litfaß Column
 - *Simulation Tools*: Modelica
 - *Planning and Optimization*: constraint programming
- Intelligent Data Analysis (IDA)
 - Brain-Computer Interface
- Embedded Systems (EST)
 - *Software Quality*: Testing, Analysis, and Consulting
 - *Customized Architectures*: Dependable Systems, Fault Tolerance, Dependable Middleware



Embedded Systems – Our Team

- We bring over 20 years experience in the design and the evaluation of complex IT systems.
- Hands-on Experience
 - Team comprised of 30 scientists/engineers
 - Full spectrum: Developers, Analysts, & Subject Area Experts
- Scientific Experts
 - Institute Head: Prof. Jähnichen, *Software Technology* Chair at **TU Berlin**
 - Chief Scientist: Prof. Schlingloff, *Specification, Verification and Test Theory* Chair at **Humboldt University Berlin**
 - Senior Consultant: Prof. Behr, *Computer Architecture*, at **Potsdam University**



Customized Architectures

Dependable Systems

- Architectures for Intelligent Electronic Control Systems for Space, Rail, Automation and Medical Applications

Project Examples

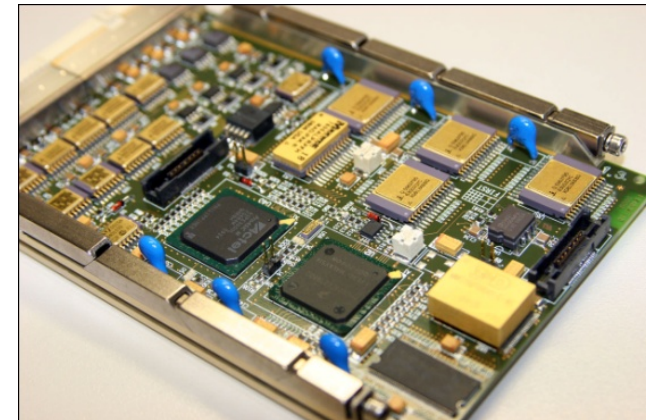
- Development of a Scalable Failsafe Robot Control System for Space Missions (RESROP)
- Development and Implementation of Space Control System (BIRD, TET)
- Lottery Computer (KENO)



TET Hardware

TET-1 SBC

- Multi computer system with identical processing nodes
- Parallel nodes provide fault tolerance
- Redundant I/O and communication structure
- Two active nodes (master/monitor) two cold sparing nodes
- PPC 823, 48 MHz, 64 MByte
- Temperature range -40 to +85°C

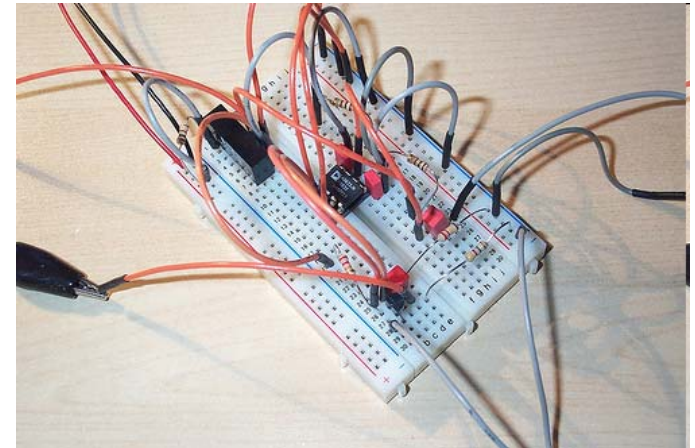


BOSS Operating System

BOSS OS

- Light weight threads
- Integrated event management
- RT functions
- Device API
- Framework for applications

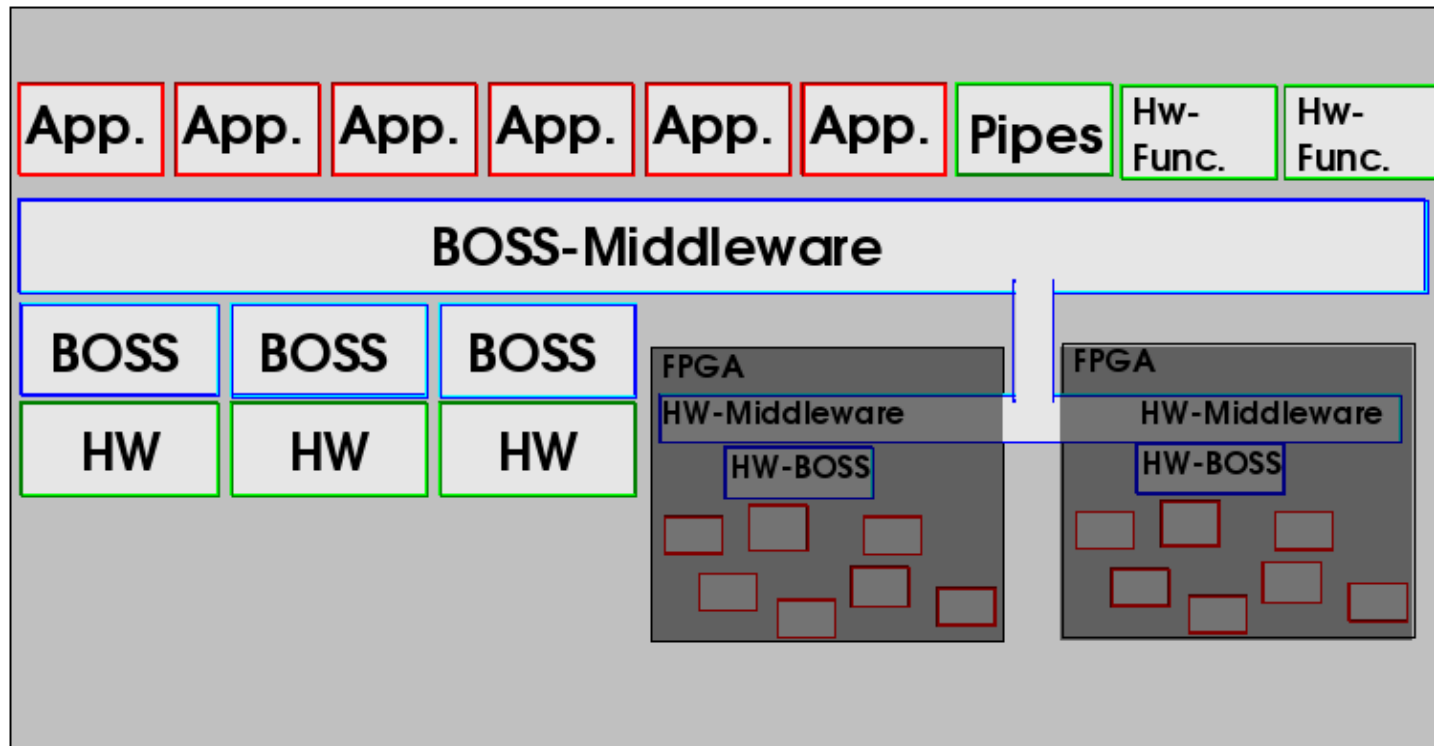
Goal: Multi-Core



TET: Hardware BOSS

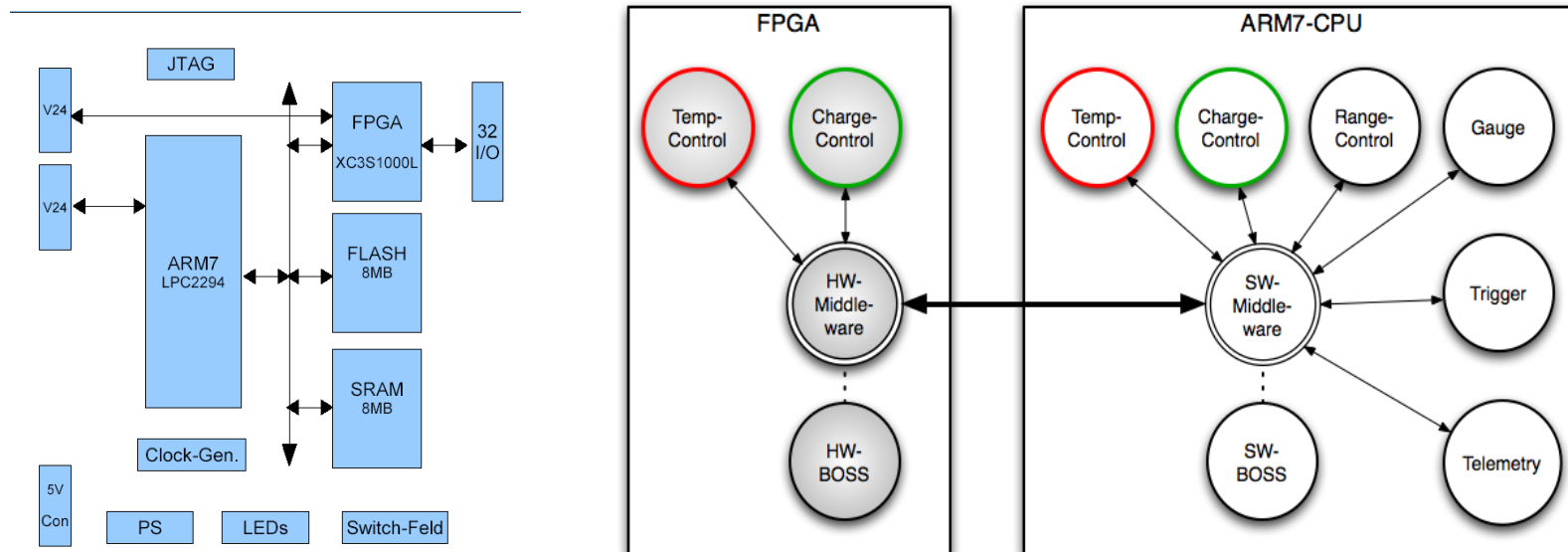
FPGA HW BOSS

- Dedicated BOSS OS functions implemented in Hardware
- Increased performance, decreased power consumption
- True parallel execution, minimal response time
- More flexibility in system design
- Hardware as a service
- Smart migration and development path: HW BOSS extends RT OS BOSS



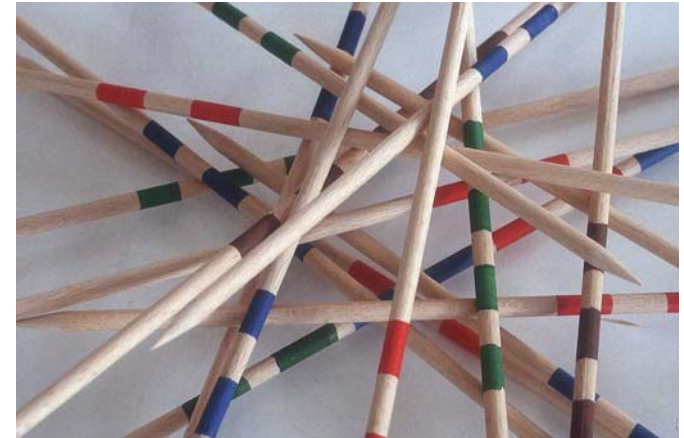
HW BOSS: Demonstration

- combined system of ARM7-CPU and Spartan3-FPGA
- application running on combined system
- collecting data on behaviour in space



Summary

- TET SBC is a PPC based architecture
 - derived from the COTS based BIRD SBC
- BOSS OS will evolve towards Multi-Core CPUs
- HW BOSS is the extension of BOSS to a HW/SW co-acting OS layer
 - flexible system design and representation
 - smooth development path for FPGA based functionalities



Many thanks for your attention!

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